US-PAT-NO: 5920775

DOCUMENT-IDENTIFIER: US 5920775 A

TITLE: Method for forming a storage capacitor within an integrated circuit

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Detailed Description Text - DETX (22):

Although capacitor dielectric layers may in general be formed of several dielectric materials, including but not limited to silicon oxides, silicon nitrides and silicon oxynitrides, higher performance capacitors are typically and preferably formed with capacitor dielectric layers formed from dielectric materials of higher permittivity, such as, but not limited to, tantalum oxide (Ta_2O_5), lead-zirconium titanates ($(Pb,Zr)TiO_3$) (PZT), and barium-strontium titanates ($(Ba,Sr)TiO_3$). Layers of such higher permittivity dielectric materials may be formed through methods including but not limited to Physical Vapor Deposition (PVD) sputtering methods, Chemical Vapor Deposition (CVD) co-deposition methods and thermal oxidation methods, as is appropriate to the high permittivity dielectric material. For the preferred embodiment of the method of the present invention, the patterned storage capacitor dielectric layer 34 is preferably formed of either tantalum oxide (Ta_2O_5), a

SOI

US-PAT-NO: 6376332

DOCUMENT-IDENTIFIER: US 6376332 B1

TITLE: Composite member and separating method therefor, bonded substrate stack and separating method therefor, transfer method for transfer layer, and SOI substrate manufacturing method

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Brief Summary Text - BSTX (5):

A substrate (SOI substrate) having an SOI (Silicon On Insulator) structure is known as a substrate having a single-crystal Si layer on an insulating layer. A device using this SOI substrate has many advantages that cannot be achieved by ordinary Si substrates. Examples of the advantages are as follows.

US-PAT-NO: 6432793

DOCUMENT-IDENTIFIER: US 6432793 B1
See image for Certificate of Correction

TITLE: Oxidative conditioning method for metal oxide layer and applications thereof

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Brief Summary Text - BSTX (5):

A capacitor, in its simplest form, consists of two conducting electrode surfaces separated by an insulating dielectric material. In the early development of the semiconductor capacitor, a doped substrate was used as the first electrode, silicon dioxide was used as the dielectric material, and a metal layer was used as the second electrode. More recently, and due to technological advances, the capacitor electrodes are now commonly made from materials such as polysilicon, epitaxial silicon, silicides, salicides, as well as several metals including osmium, rhodium, platinum, gold, ruthenium, and aluminum, while the capacitor dielectric is now commonly made from materials such as oxide-nitride-oxide (ONO), tantalum pentoxide, and lead zirconium titanate.

US-PAT-NO: 5527724

DOCUMENT-IDENTIFIER: US 5527724 A

TITLE: Method to prevent latch-up and improve breakdown volatge in SOI mosfets

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Brief Summary Text - BSTX (3):

Circuits and devices built in SOI substrates have been shown to have many advantages over identical circuits built in bulk silicon substrates. SOI (silicon-on-insulator) technology has been touted as a promising approach for fabricating advanced integrated circuits because of its faster speed and improved radiation tolerance. However, one of the disadvantages of SOI devices is the parasitic bipolar induced latch-up/breakdown voltage, which severely limits the maximum power supply voltage at which SOI circuits and devices can operate. When the parasitic device turns on, the SOI device cannot be switched off by changing its gate bias. This single transistor latch-up also manifests itself as a very low breakdown voltage. The SOI device self latch-up effect is caused by a positive feedback mechanism generated by the steady-state balancing between the minority and majority carriers in the body of the transistor. For a given gate voltage, as the drain voltage is increased, the electric field at

the body/drain junction becomes high enough so that electron/hole pairs are generated by impact ionization. The majority carriers (carriers of the same dopant type as the source and drain) are collected at the drain while minority carriers travel into the body of the transistor. In SOI devices, the body of the transistor is separated from the substrate by a buried oxide. The minority carriers thus collect in the body of the transistor. At sufficiently high drain bias, the concentration of minority carriers in the body disturbs the normal steady state potential of the body. To compensate, majority carriers are injected from the source. These carriers then diffuse to the high field region of the drain/body junction, creating even more electron/hole pairs by impact ionization, and cause a run-away current in the device.